IN THE SPECIFICATION:

Paragraph beginning at line 3 of page 1 has been amended as follows:

The present invention relates to a switched capacitor amplifier circuit that cancels an offset voltage and to an electronic device ~~using~~ equipped with the switched capacitor amplifier circuit.

Paragraph beginning at line 11 of page 2 has been amended as follows:

The input offset voltage of the operational amplifier is charged in the capacitors 101 and 102 in the reset phase f1. A variation in the potential between both ends of the capacitor 101 in the sampling phase f2 is a difference between the voltage of the input terminal 141 and the standard voltage given to the switch 123. Similarly, a variation in the potential between both ends of the capacitor 102 in the sampling phase f2 is a difference between the voltage of the input terminal 142 and the standard voltage given to the switch 124. Accordingly, ~~The~~ the variation in the voltage charged between both ends of the capacitors 101 and 102 becomes a difference between the input voltage and the standard voltage, and the offset voltage is not included in

the variation. For that reason, the offset voltage of the operational amplifier is not ~~amplified,~~ amplified and cancelled.

Paragraph beginning at line 6 of page 4 has been amended as follows:

Hereinafter, a preferred embodiment of the present invention will be described with reference to the accompanying drawings. Fig. 1 is an example of the structural diagram of the switched capacitor amplifier circuit in accordance with the present invention. In Fig. 1 reference numerals 101, 103, 102 and 104-106 show first-sixth capacitors, respectively, reference numerals 127, 131, 123, 121, 124, 122, 125, 126, 129, 130, 128 and 132 show first-twelfth switch circuits, respectively, and reference numerals 111 and 112 are nodes at which first and second reference voltages are obtained. In the reset phase f1, the switch circuit 123 is closed, the capacitor 101 is connected to a node 111, the switch circuit 124 is closed, and the capacitor 102 is connected to a node 112. At the same time, the switch circuits 125 and 129 are closed, and the electric charges in the capacitors 103 and 104 are discharged. After a given period of time, the switch circuits 123, 124, 125 and 129 are opened, to thereby complete

the reset phase f1. The electric charges charged in the capacitor 101 in the reset phase f1 are represented as follows:

$$q = C1 * VREF$$

Paragraph beginning at line 14 of page 7 has been amended as follows:

In Fig. 1, some of the resistors that ~~constitutes~~ constitute the resistor 161 are connected in parallel with the switch, and the switch is opened/closed on the basis of data written in a storage device, thereby being capable of obtaining a desired voltage.

Paragraph beginning at line 18 of page 7 has been amended as follows:

~~The~~ Thus, according to the present invention, the offset voltage of the input voltage is cancelled at the low noise, and only the signal component can be amplified.